SYSTEM

Technical Information

PCL-CAPELLA

Mezzanine I/O Expansion Board (Side Card)

CFast™ Storage • 4 x GbE Rear I/O

Edition 8

Document No. 7278 • 15 August 2014

Contents

About this Manual

This manual is a short form description of the technical aspects of the PCL-CAPELLA, required for installation and system integration. It is intended for the advanced user only. The latest version of this document may be obtained from www.ekf.com/p/pcl/pcl_ti.pdf.

Edition History

Ed.	Contents/Changes	Author	Date
1	Technical Information PCL-CAPELLA, english, preliminary edition Text #7278, File: pcl_ti.wpd	jj	3 March 2014
2	Updated pin assignment rear I/O connectors J1, J2	mib	24 March 2014
3	Updated illustrations	jj	24 March 2014
4	Updated PCIe settings for carrier board	mib	7 July 2014
5	MTBF added	mib	10 July 2014
6	Photos added PCL-0100 & PCL-0200	jj	29 July 2014
7	Photo added PC3-PCL exploded view	jj	11 August 2014
8	Added restrictions for use with SC1-ALLEGRO as carrier Board	mib	15 August 2014

Related Documents

Related Information PCL-CAPELLA	
PCL-CAPELLA Home	www.ekf.com/p/pcl/pcl.html
PCL-CAPELLA Technical Information (this document, latest revision)	www.ekf.com/p/pcl/pcl_ti.pdf

Related Documents CompactPCI® PlusIO & CompactPCI® Serial	
CompactPCI® PlusIO & Serial Technology Overview	www.ekf.com/s/smart_solution.pdf
CompactPCI® PlusIO Home	www.ekf.com/p/plus.html
CompactPCI® Serial Home	www.ekf.com/s/serial.html

Nomenclature

Signal names used herein with an attached '#' designate active low lines.

Trade Marks

Some terms used herein are property of their respective owners, e.g.

- Core™ i*: ® Intel
- CompactPCI, CompactPCI PlusIO, CompactPCI Serial: ® PICMG
- Windows: ® Microsoft
- EKF, ekf system: ® EKF

EKF does not claim this list to be complete.

Legal Disclaimer - Liability Exclusion

This manual has been edited as carefully as possible. We apologize for any potential mistake. Information provided herein is designated exclusively to the proficient user (system integrator, engineer). EKF can accept no responsibility for any damage caused by the use of this manual.

Standards

Reference Documents		
Term	Document	Origin
CFast™	CFast™ Specification Rev. 2.0, 12/04/2012	www.compactflash.org
CompactPCI®	CompactPCI Specification, PICMG® 2.0 R3.0, Oct. 1, 1999	www.picmg.org
CompactPCI® PlusIO	CompactPCI PlusIO Specification, PICMG® 2.30 R1.0, November 11, 2009	www.picmg.org
CompactPCI® Serial	PICMG® CPCI-S.0 R1.0, March 2, 2011	www.picmg.org
Ethernet	IEEE Std 802.3, 2000 Edition	standards.ieee.org
LPC	Low Pin Count Interface Specification, Revision 1.1	developer.intel.com/design/chipsets/industry/lpc.htm
Micro SATA	SFF-8144 Specification	ftp://ftp.seagate.com/sff
mSATA	Jedec MO-300B mSATA SSD Assembly	www.jedec.org
PCI Express®	PCI Express® Base Specification 3.0	www.pcisig.com
PCI Express® Mini Card	PCI Express® Mini Card Electromechanical Specification	www.pcisig.com
SATA	Serial ATA Specification Rev. 3.2, August 2013	www.sata-io.org
USB	USB 2.0 Universal Serial Bus Specification	www.usb.org

Features

Feature Summary

- **3U/4HP Mezzanine Side Card** for EKF CompactPCI® PlusIO CPU boards, typically delivered as 8HP front panel width assembly together with suitable CPU carrier board, provides removable mass storage options and enhances the rear I/O functionality of the host CPU (RIO not compliant with CompactPCI® Serial CPU carrier cards)

- **Front panel I/O** (available for both CompactPCI® PlusIO and CompactPCI® Serial CPU carrier cards
- Removable SATA based SSD mass storage device (front panel slot), choice between two form factors (ordering alternates)
- PCL-0100-CAPELLA: Suitable for a removable CFast™ card
- PCL-0200-CAPELLA: Suitable for a removable Micro SATA SSD 1.8-inch
- 2 x USB 2.0 F/P connectors

- **On-Board Storage Options**
- Available for both CompactPCI® PlusIO and CompactPCI® Serial CPU carrier cards (Serial CPU Cards w/o Rear I/O)
- Option on-board mSATA module host connectorerian CPU
- Option on-board secondary CFast™ card host connector

- **Rear I/O option J1/J2**
- Available for CPCI PlusIO CPU carrier boards only, not available with CompactPCI® Serial CPU carrier cards
- 4 x Gigabit Ethernet ports (4 x Intel® 82574IT networking interface controllers)
- 2 x SATA channels
- 4 x USB 2.0 ports
- 4 x UART (TTL), KB/MS, GPIO

- **Environment & Regulation**
- Long term availability
- Coating, sealing, underfilling on request
- RoHS compliant 2002/95/EC
- Operating temperature: 0°C to +70°C (industrial temperature range on request)
- Storage temperature: -40°C to +85°C, max. gradient 5°C/min
- Humidity 5% ... 95% RH non condensing
- Altitude -300m ... +3000m
- Shock 15g 0.33ms, 6g 6ms
- Vibration 1g 5-2000Hz
- MTBF 159.7 years
- EC Regulations EN55022, EN55024, EN60950-1 (UL60950-1/IEC60950-1)

General Information

*Available as a mezzanine add-on expansion board (aka side board) to CompactPCI® PlusIO CPU cards, the **PCL-CAPELLA** provides front panel removable mass storage, suitable for either a CFast™ card or a Micro SATA 1.8-inch SSD (ordering options). Either a CFast™ card or mSATA module can be populated on-board in addition.*

The PCL-CAPELLA offers a rich suite of rear I/O functions via the J1/J2 connectors, e.g. 4 x Gigabit Ethernet (NIC), 2 x SATA, 4 x USB, and 4 x UART. EKF offers rear I/O module design tailored to the customer needs. The PCL-CAPELLA can be used also together with CompactPCI® Serial CPU cards, but RIO is available exclusively for CompactPCI® PlusIO carrier cards.

PCL-0100-CAPELLA (8HP Assembly w. PC3-ALLEGRO CPU Card)

PCL-0100-CAPELLA CFast™ Slot Released

PCL-0100-CAPELLA CFast™ Slot Locked

PCL-0100-CAPELLA

PCL-0200-CAPELLA

PCL-0200-CAPELLA uSATA Slot Released

PCL-0200-CAPELLA uSATA Slot Locked

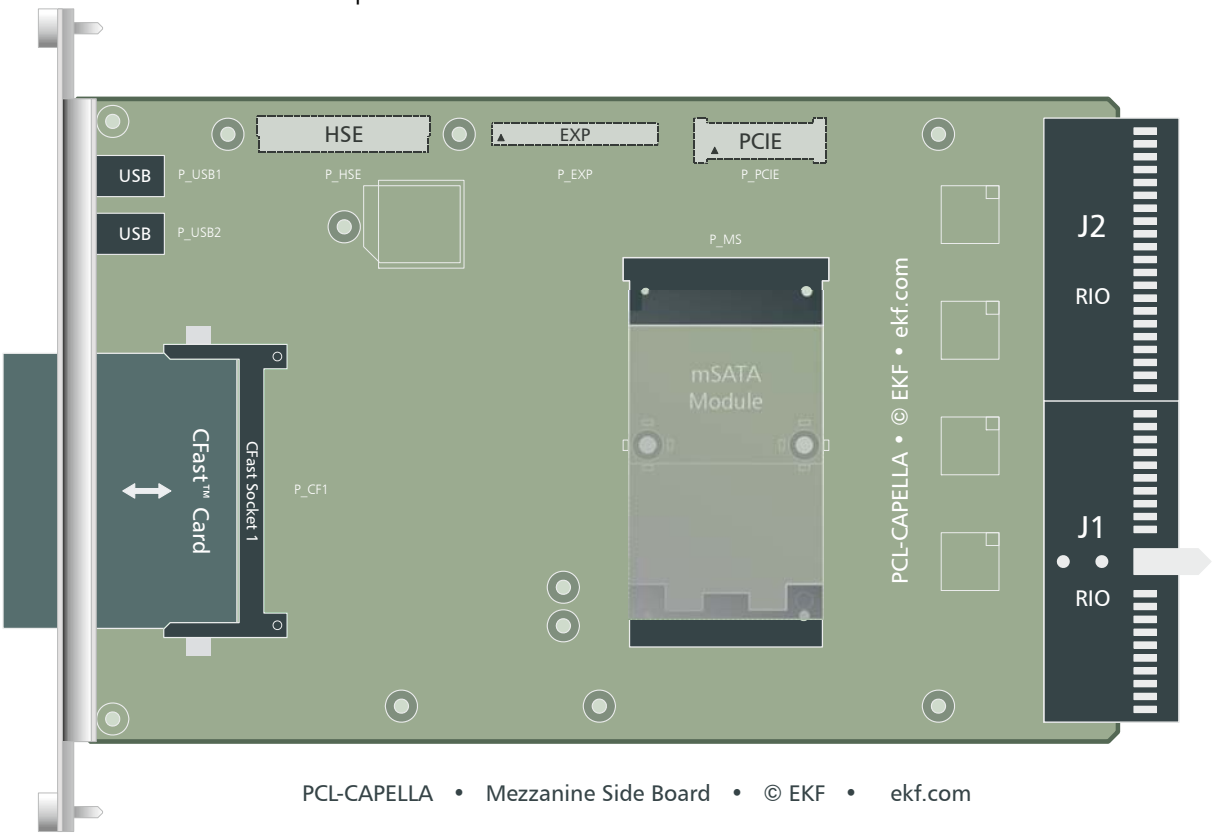
System Requirements

The PCL-CAPELLA is a mezzanine side card, to be fixed on top of a suitable CPU carrier board. The pitch between carrier PCB and mezzanine PCB is 4HP, resulting in a 8HP common front panel for the entire assembly.

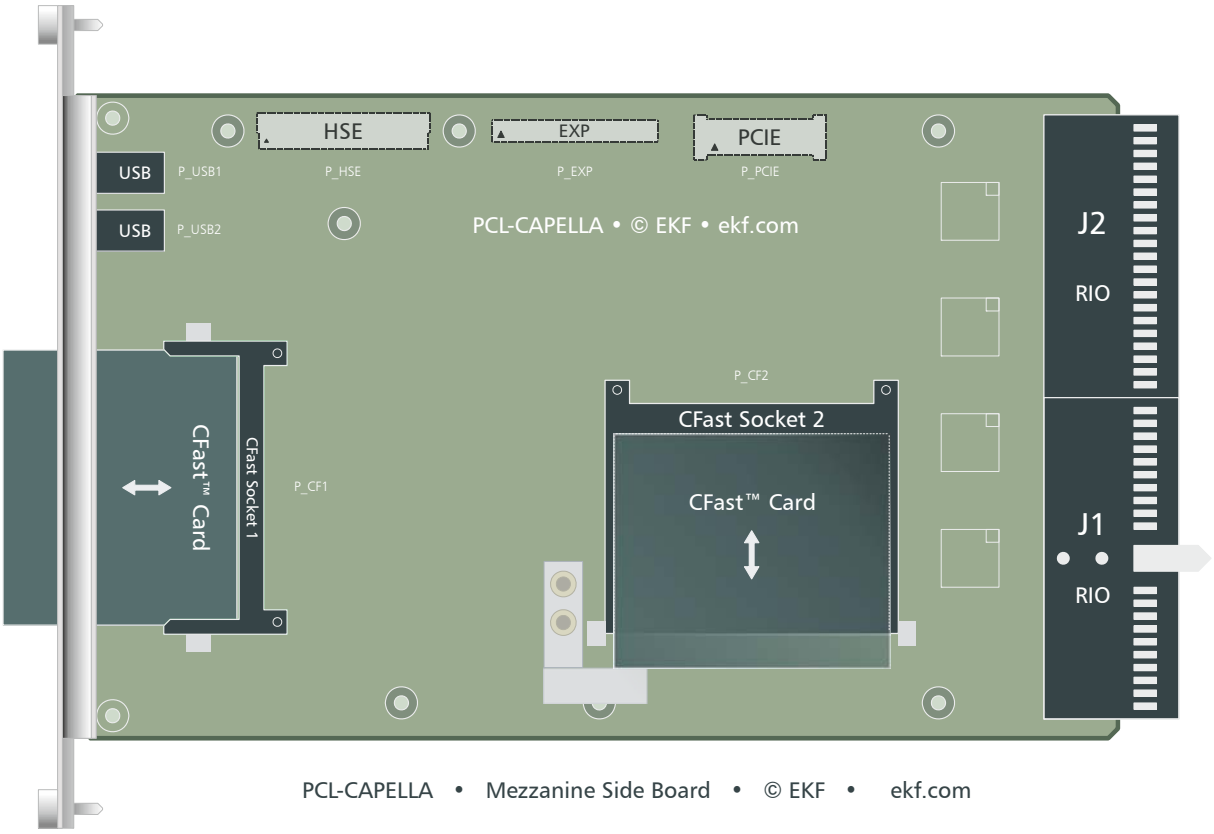
Up to three mezzanine inter-board connectors are in use, for distribution of legacy and high speed I/O signals from the CPU carrier to the side board. These are referred to as *HSE* (SATA & USB 2.0 High Speed Expansion), *EXP* (Legacy Expansion), and *PCIE* (PCI Express® x 4). The mezzanine connectors are situated on the bottom side of the PCL-CAPELLA, facing towards their mating CPU card connectors.

With respect to the system backplane, it is recommended to have the CPU card system slot on the right edge, in order to prevent loss of a peripheral slot (the PCL-CAPELLA is then positioned out of backplane shape). The rear I/O option requires a single slot P1/P2 RIO backplane or similar custom solution in addition, and is available with CompactPCI® PlusIO CPU carrier cards only, such as the PC1-GROOVE and PC3-ALLEGRO. Rear I/O is not available with a CompactPCI® Serial CPU carrier, since the CPCI Serial backplane connector suite (CPU system slot) would slightly overlap the hard metric P1/P2 connectors as required for the PCL RIO backplane.

Mezzanine Connectors (HSE, EXP, PCIE)
Option on-Board mSATA Module Socket

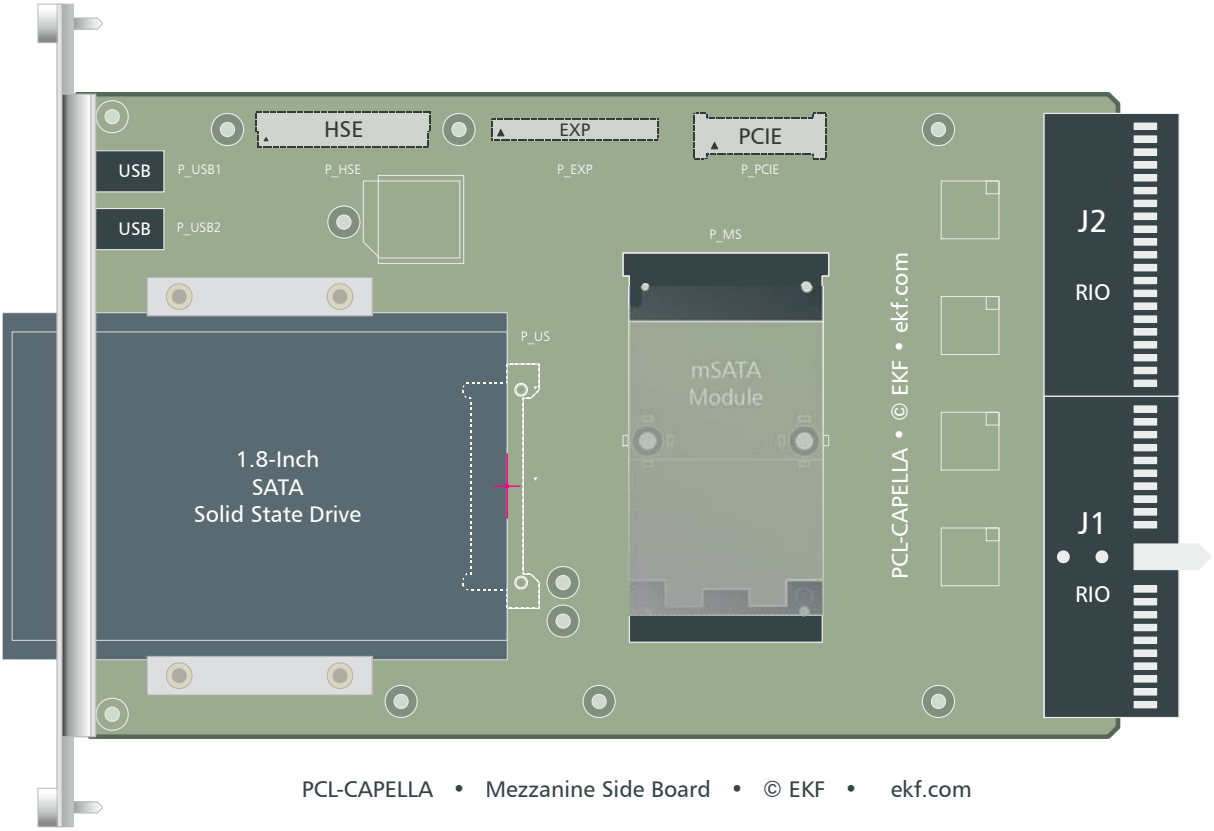


PCL-CAPELLA • Mezzanine Side Board • © EKF • ekf.com



PCL-CAPELLA • Mezzanine Side Board • © EKF • ekf.com

Option Dual CFast™ Card Sockets



PCL-CAPELLA • Mezzanine Side Board • © EKF • ekf.com

Option F/P µSATA SSD Socket

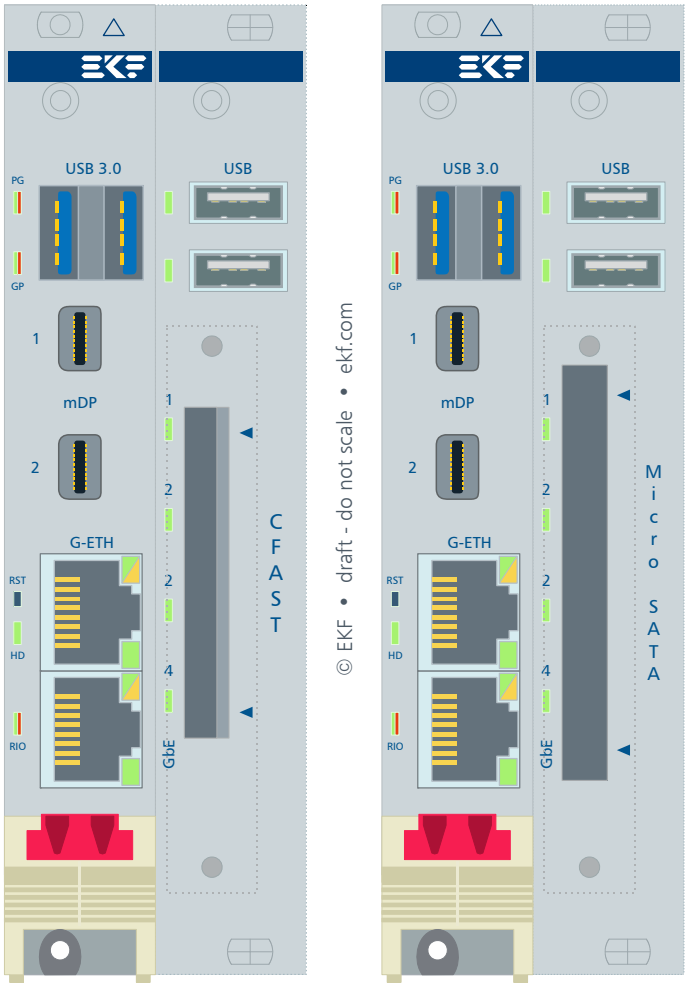
Front Panel I/O

The PCL-CAPELLA expands the suite of front panel connectors of a particular CPU carrier board by two USB 2.0 receptacles and a card slot suitable for either a CFast™ card (SATA based SSD storage module), or 1.8-inch size micro SATA SSD (ordering options).

The front panel removable device (either type) can be fixed by a screw locked latch.

Rear I/O Ethernet link/activity status is signalled via the front panel, in addition to the front panel USB power state.

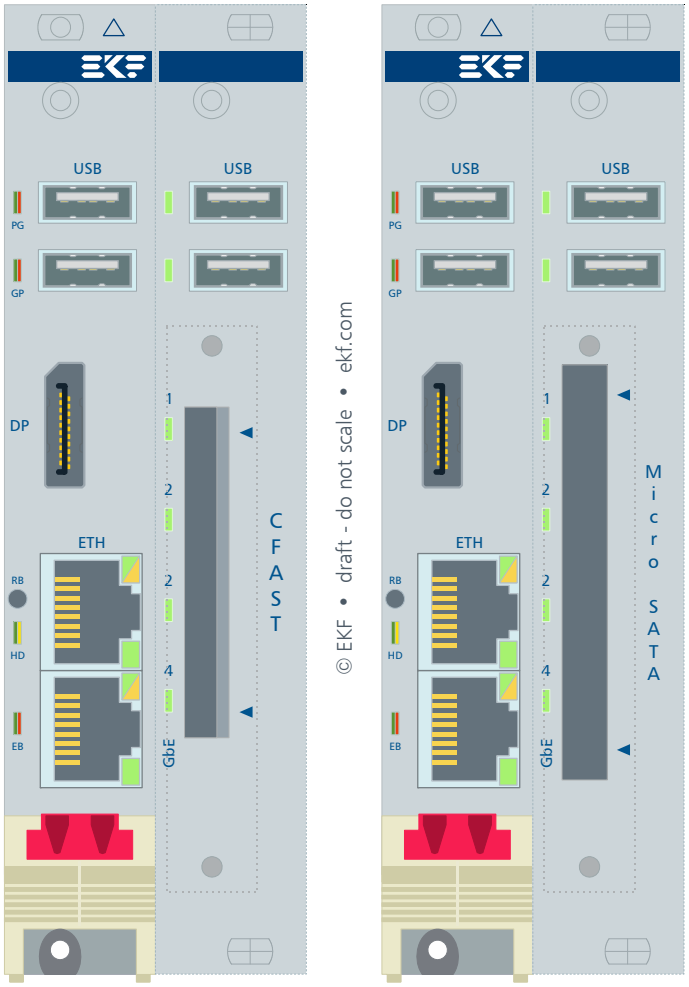
Front Panel Options (w. PC3-ALLEGRO)



PC3-ALLEGRO Dual - mDP | PCL-CAPELLA CFast™

PC3-ALLEGRO Dual - mDP | PCL-CAPELLA μ SATA

Front Panel Options (w. PC1-GROOVE)



PC1-GROOVE DisplayPort | PCL-CAPELLA CFast™

PC1-GROOVE DisplayPort | PCL-CAPELLA μ SATA

PCL-0100-CAPELLA Front Panel - CFast™ Slot Open and Locked

PCL-0200-CAPELLA Front Panel - uSATA Slot Open and Locked

Theory of Operation

The PCL-CAPELLA side board communicates by means of three bottom mount expansion connectors with the host CPU: *PCIE* (PCI Express x 4), *HSE* (High Speed Expansion meaning SATA and USB), and *EXP* (multi-function legacy I/F such as LPC). Best results can be achieved with the PC1-GROOVE or PC3-ALLEGRO as CPU carrier card. Older CPU cards may not support all the functions available on the PCL-CAPELLA.

The PCI Express® interface mezzanine connector *PCIE* is comprised of 4 PCIe links/lanes. The CPU carrier must be configured for 4 links x 1 (by CPU card DIP-switch settings, consult CPU user guide). On the PCL-CAPELLA, each PCIe lane is wired to a dedicated PCIe Gigabit Ethernet controller, for rear I/O usage via the backplane connector J1.

The *HSE* mezzanine connector passes a maximum of 4 x SATA channels and 4 x USB 2.0 ports from the host CPU to the PCL-CAPELLA side board. Two SATA channels are assigned to the front panel removable SSD (port 1, SATA 3G), and the on-board CFast™ card socket (port 4, SATA 3G). Another two SATA channels are reserved for rear I/O via on-board redrivers (port 2 & 3, SATA 6G). Since the J1/J2 hard metric connectors are not specified for high speed differential signalling, SATA 6G cannot guaranteed for rear I/O (fall back to 3G).

Two of the USB 2.0 ports passed from the mezzanine connector *HSE* are wired to USB front panel receptacles across a TPS2060 USB power switch, as overcurrent and short-circuit protection. Front panel LEDs are provided to signal the power state of the assigned front panel USB receptacles. The remaining two USB ports from HSE are available for rear I/O.

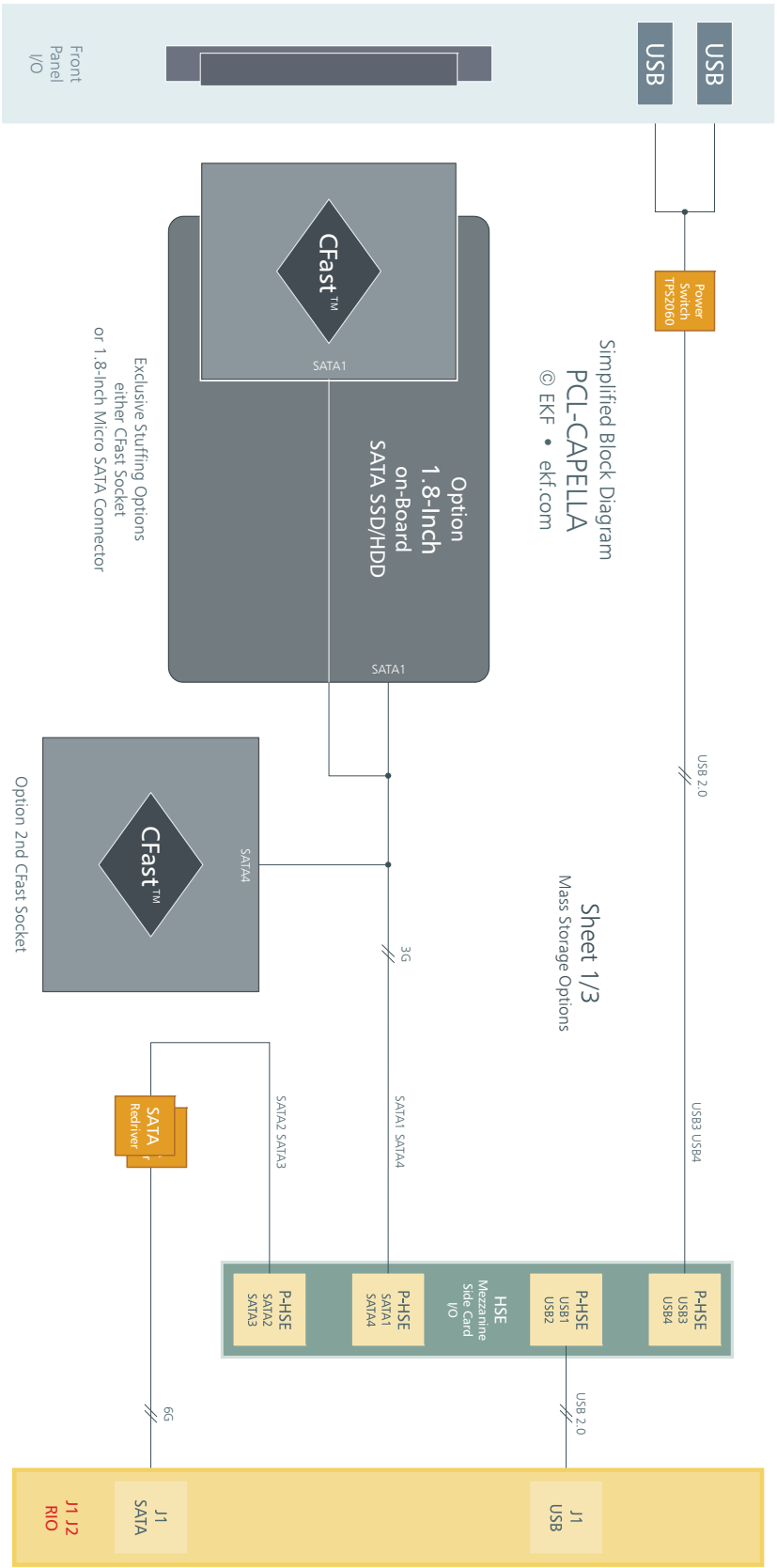
The mezzanine connector *EXP* combines several side-band data channels. The LPC (Low Pin Count) enables an on-board super-I/O (SIO) controller chip to emulate the legacy I/O interfaces; among these are the classic serial UART (COM) and PS/2 keyboard/mouse ports.

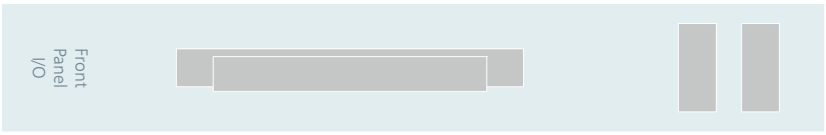
Another two USB ports derived from *EXP* are passed to the backplane connector J2 for rear I/O. An on-board I2C EEPROM is tied to the SMbus.

The PCL-CAPELLA side board accommodates one or two SATA based mass storage devices. While the on-board CFast™ card socket is recommended as boot device, the front panel CFast™ card or 1.8-inch Micro SATA SSD may be used as removable data storage.

Please note, that ‘removable’ throughout this document does not mean ‘hot swap’. In order to avoid data loss or even damage to a storage device, shut down the system regularly and disconnect power before replacing the front panel SSD.

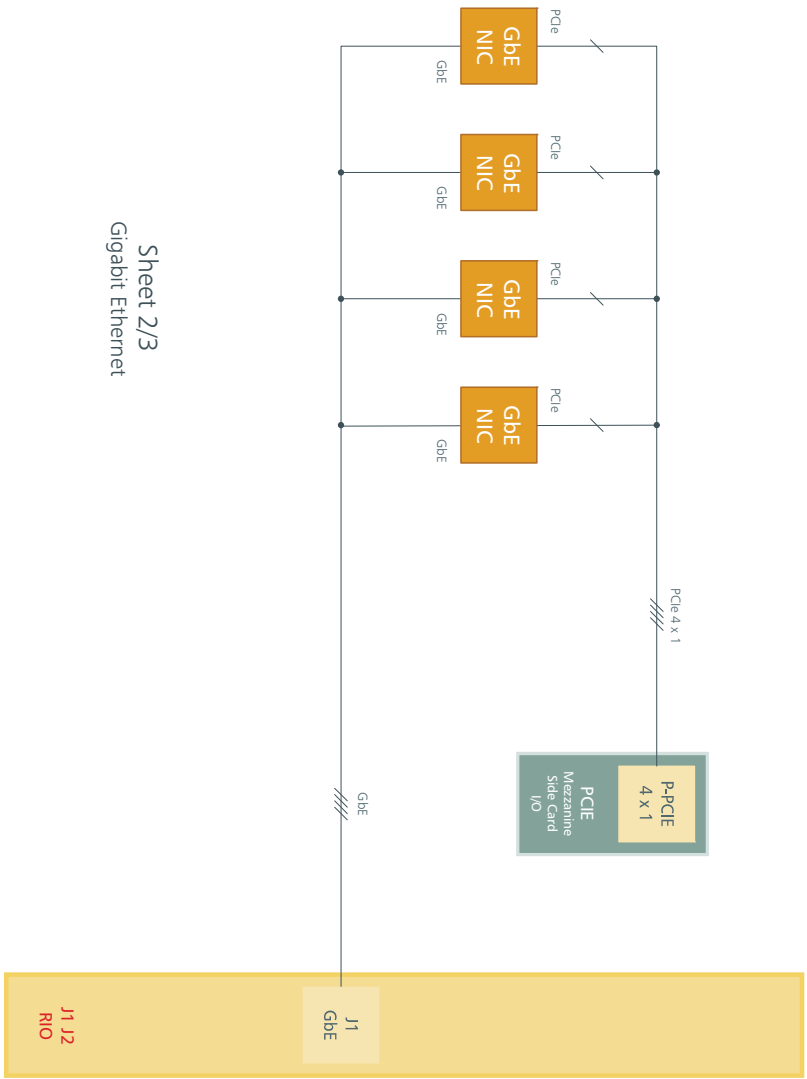
Block Diagram

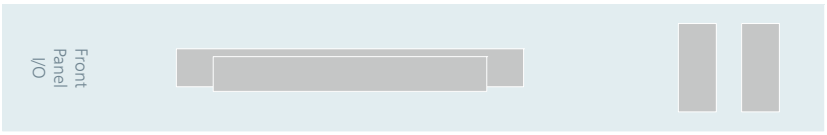




Simplified Block Diagram
PCL-CAPELLA
© EKF • ekf.com

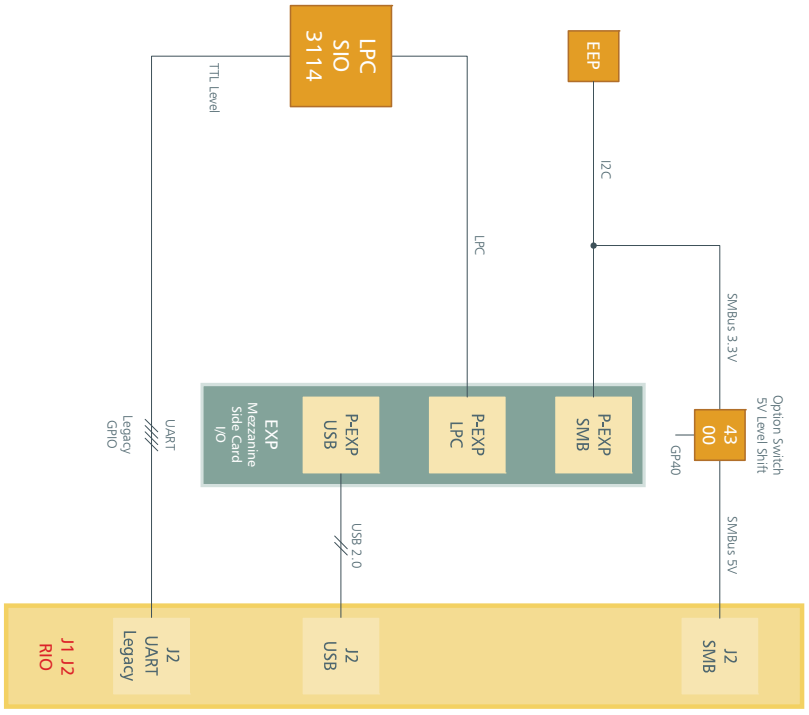
Sheet 2/3
Gigabit Ethernet





Simplified Block Diagram
PCL-CAPELLA
© EKF • ekf.com

Sheet 3/3
UART/Legacy



Summary of Connectors

Not all of the connectors or other elements listed below may be present or functional on your actual PCL-CAPELLA board. Assembly of these connectors is highly custom specific. Discuss your needs (target application) with EKF before ordering, for an optimum CPU & side card configuration.

Front Panel Connectors

CF1	CFast™ card host connector, for a front panel removable SSD (PCL-0100 ordering option)
US1	Micro SATA SSD host connector, for a front panel removable SSD (PCL-0200 ordering option)
USB	USB 2.0 receptacles

On-Board Connectors

CF2	CFast™ card host connector, for a secondary CFast™ SSD (ordering option, exclusive to MSATA1)
MS1	mSATA module host connector, for a mSATA SSD module (ordering option, exclusive to CF2)

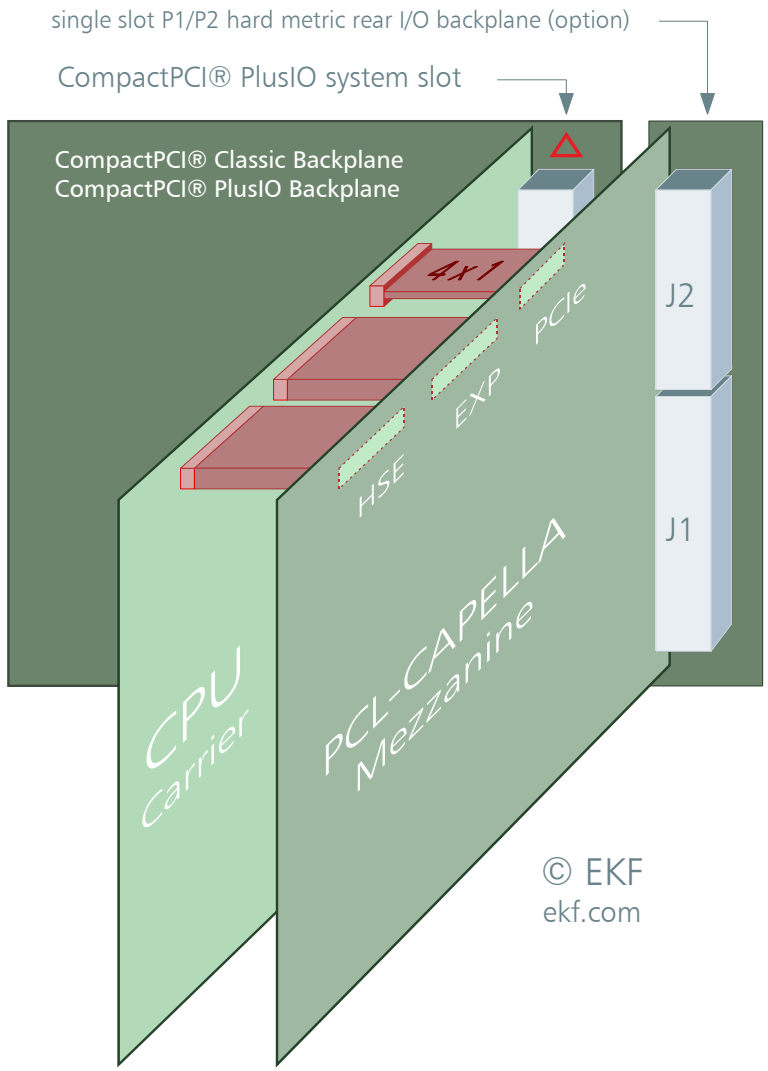
Inter-Board Connectors (CPU Carrier)

EXP	Dual row socket, available from bottom of the PCL-CAPELLA PCB, mating with the corresponding socket on the CPU carrier board, connected through a board stacker, comprised of: ▸ LPC Low Pin Count interface ▸ 2 x USB ▸ SMB, Speaker, Reset
HSE	High speed mezzanine connector, available from bottom of the PCL-CAPELLA PCB, mating with the corresponding connector on the CPU carrier board, comprising of: ▸ Host CPU (PCH) SATA 3G (SATA1 & SATA4 ports) ▸ Host CPU (PCH or 88SE9170) SATA 6G (SATA2 & SATA3 ports) ▸ Host CPU 4 x USB
PCIE	High speed socket edge card connector, available from bottom of the PCL-CAPELLA PCB, mating with the corresponding socket on the CPU carrier board, connected through a high speed strip line PCB (C22), comprising of: ▸ Host CPU PCI Express (PCIe) x 4 interface (must be configured as 4 links x 1 lane)

Rear I/O Connectors

J1	Rear I/O option 2.00mm brown keyed hard metric female connector ▸ 4 x Gigabit Ethernet ports, derived from on-board PCIe networking interface controllers ▸ SATA2 & SATA3 channels derived from the HSE mezzanine connector ▸ 2 x USB 2.0 derived from the HSE mezzanine connector
J2	Rear I/O option 2.00mm hard metric female connector ▸ 4 x GPIO derived from SIO ▸ LPT parallel port ▸ Serial ports (UART TTL-level signals) ▸ 2 x USB 2.0 derived from the EXP mezzanine connector ▸ PS/2 keyboard & mouse ▸ SMBus, Speaker, Reset#

Backplane Mounting



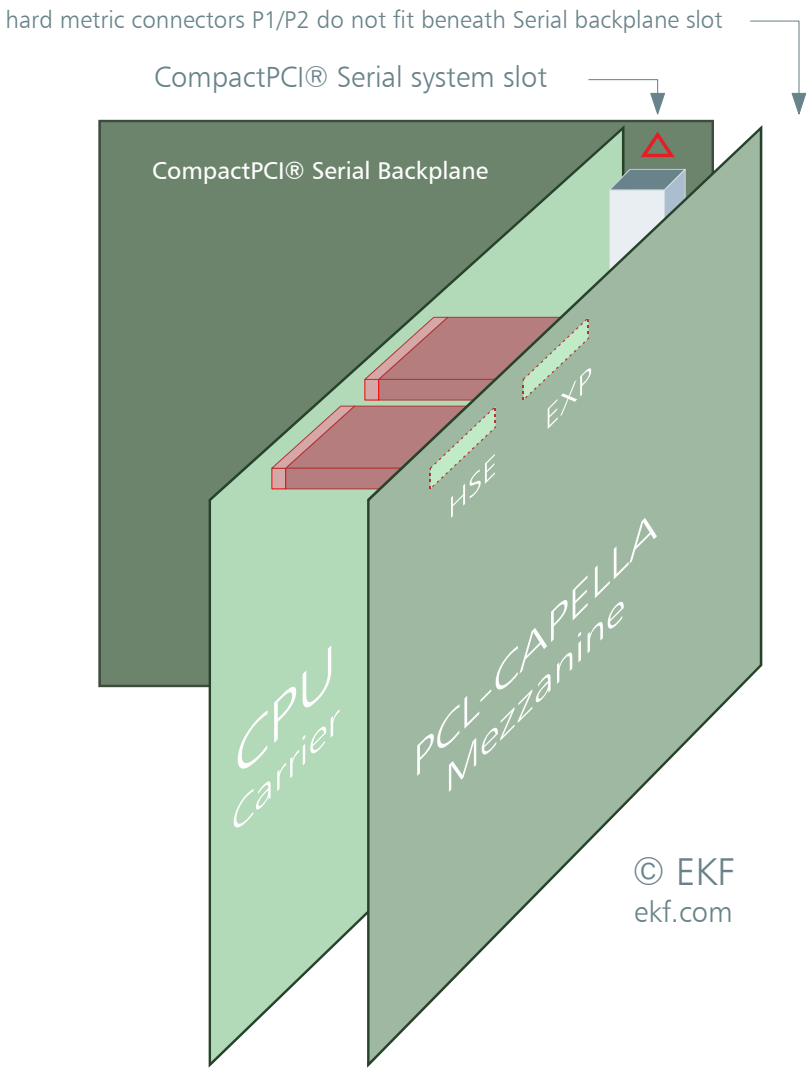
RIO option with CompactPCI® PlusIO

The PCL-CAPELLA can be used as an assembly together with a CompactPCI® PlusIO CPU carrier card such as the PC3-ALLEGRO. If used together with a CompactPCI® Serial CPU board such as the SC1-ALLEGRO, no rear I/O connectors can be stuffed for mechanical reasons.

If the backplane is provided with a right aligned system slot, be sure to position the CPU carrier board to the system slot (and not the PCL-CAPELLA). Consequently, the PCL-CAPELLA then occupies the next card cage slot to the right, outside of the backplane shape.

This assembly order (right aligned backplane system slot) is recommended because no regular CompactPCI® or CompactPCI® Serial backplane peripheral slot would get lost for the PCL-CAPELLA.

A single slot rear I/O P1/P2 backplane would be required in addition in order to make use of the rear I/O capability of the PCL-CAPELLA. With J1/J2 stuffed, a coding key present on J1 would prevent insertion of the PCL-CAPELLA into a regular CompactPCI® card slot. J1/J2 cannot be used with a CPCI Serial CPU carrier card.



RIO option not available w. CompactPCI® Serial

Combined with a CompactPCI® Serial CPU carrier card, the PCL-CAPELLA cannot be used for rear I/O. The hard metric P1/P2 connectors on a single slot RIO backplane would collide with the left hand high speed CPCI Serial Airmax backplane connectors J1-J6, for a nominal 4HP slot pitch. This issue is addressed in the CPCI-S.0 specification, chapter 5.3.

Together with a CompactPCI® Serial CPU carrier card assembly, the PCL-CAPELLA will not be populated with connectors and components which are assigned to rear I/O only. The PCL-CAPELLA would be restrained to removable front panel SSD storage and the on-board CFast™ card in this application.

Installing and Replacing Components

Before You Begin

Warnings

The procedures in this chapter assume familiarity with the general terminology associated with industrial electronics and with safety practices and regulatory compliance required for using and modifying electronic equipment. Disconnect the system from its power source and from any telecommunication links, networks or modems before performing any of the procedures described in this chapter. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage. Some parts of the system can continue to operate even though the power switch is in its off state.

Caution

Electrostatic discharge (ESD) can damage components. Perform the procedures described in this chapter only at an ESD workstation. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis or board front panel. Store the board only in its original ESD protected packaging. Retain the original packaging (antistatic bag and antistatic box) in case of returning the board to EKF for repair.

Installing the Board

Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system 
- Remove the board assembly packaging, be sure to touch the board only at the front panel
- Identify the related CompactPCI slot (peripheral slot for I/O boards, system slot for CPU boards, with the system slot typically most right or most left to the backplane)
- Insert card carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- A card with onboard connectors requires attachment of associated cabling now
- Lock the ejector lever, fix screws at the front panel (top/bottom)
- Retain original packaging in case of return

Removing the Board

Warning

This procedure should be done only by qualified technical personnel. Disconnect the system from its power source before doing the procedures described here. Failure to disconnect power, or telecommunication links before you open the system or perform any procedures can result in personal injury or equipment damage.

Typically you will perform the following steps:

- Switch off the system, remove the AC power cord
- Attach your antistatic wrist strap to a metallic part of the system
- Identify the board, be sure to touch the board only at the front panel
- Unfasten any front panel screws (top/bottom), unlock the ejector lever
- Remove any onboard cabling assembly
- Activate the ejector lever
- Remove the card assembly carefully (be sure not to damage components mounted on the bottom side of the board by scratching neighboured front panels)
- Store board in the original packaging, do not touch any components, hold the board at the front panel only

Warning

Do not expose the card to fire. Battery cells and other components could explode and cause personal injury.

EMC Recommendations

In order to comply with the CE regulations for EMC, it is mandatory to observe the following rules:

- The chassis or rack including other boards in use must comply entirely with CE
- Close all board slots not in use with a blind front panel
- Front panels must be fastened by built-in screws
- Cover any unused front panel mounted connector with a shielding cap
- External communications cable assemblies must be shielded (shield connected only at one end of the cable)
- Use ferrite beads for cabling wherever appropriate
- Some connectors may require additional isolating parts

Technical Reference

Caution

Some of the connectors may provide operating voltage (e.g. +12V, +5V and +3.3V) to devices inside the system chassis, such as internal peripherals. Not all of these connectors are overcurrent protected. Do not use these connectors for powering devices external to the computer chassis. A fault in the load presented by the external devices could cause damage to the board, the interconnecting cable and the external devices themselves.

Please Note

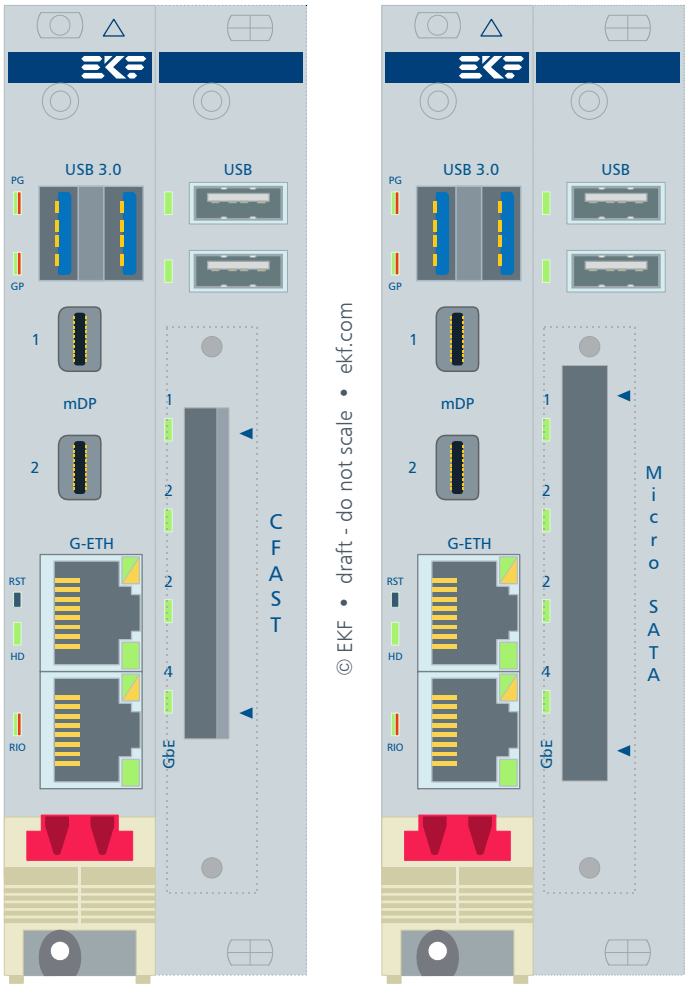
The PCL-CAPELLA mezzanine module may be equipped with several on-board connectors for system internal usage. Not all of these connectors may be present on a particular board. Be sure to specify your individual needs when ordering the PCL-CAPELLA board. Characteristic features and the pin assignments of each connector are described on the following pages (connector designation in alphabetical order within the groups 'front panel connectors', 'on-board connectors', 'inter-board connectors', and 'rear I/O connectors').

Warning

'Removable' throughout this document does not mean 'Hot Swap'. In order to avoid data loss or even damage to a storage device, shut down the system regularly and turn power off before replacing the front panel SSD.

Front Panel Elements

As of current, suitable CPU carrier boards for use together with the PCL-CAPELLA side card are the PC1-GROOVE and the PC3-ALLEGRO. The PCL-CAPELLA side board mounts on top (at the right side) of the CPU card. By default, the PCL-CAPELLA shares an 8HP (~40.6mm) front panel with the CPU. Further more, custom specific front panel options are available on request. Shown below are typical variants of the PCL-CAPELLA.



PC3-ALLEGRO Dual - mDP | PCL-CAPELLA CFast™ | PC3-ALLEGRO Dual - mDP | PCL-CAPELLA μ SATA

CFast™	Front panel slot suitable for insertion of a CFast™ card SSD
Micro SATA	Front panel slot suitable for insertion of a Micro SATA 1.8-inch SSD
USB	USB 2.0 receptacles & USB power LEDs
GbE 1-4	Gigabit Ethernet (Rear I/O only) link & activity for each of 4 networking interface controller

USB

The PCL-CAPELLA is equipped with a two front panel receptacles, which can accommodate USB 2.0 type A cable connectors (USB root hub). Both USB jacks are tied to the mezzanine connector HSE. A power switch is equipped on-board, for short circuit protection. Front panel LEDs are provided to signal USB power on.

USB Receptacles 2 x USB 2.0 type A receptacles (270.23.18.2)		
 USB 2.0 Receptacle © EKF • ekf.com • #270.20.04.3	1	VBUS +5V 1.5Amax 1)
	2	USB D-
	3	USB D+
	4	GND

1) Each connector provides +5V (VBUS) for powering external devices. A dual-channel electronic power switch (TPS2060) is used on the PCL-CAPELLA which limits the maximum output current of each individual USB connector to a safe level. The USB power switch is rated at >2A current limit typically, which is suitable even for applications where heavy capacitive loads are likely to be encountered, e.g. VBUS powered USB disk drives. The electronic switch is enabled by the CPU carrier card PCH (i.e. it is managed by the driver software). Front panel LEDs signal the power-on state individually for each USB receptacle.

CFast™

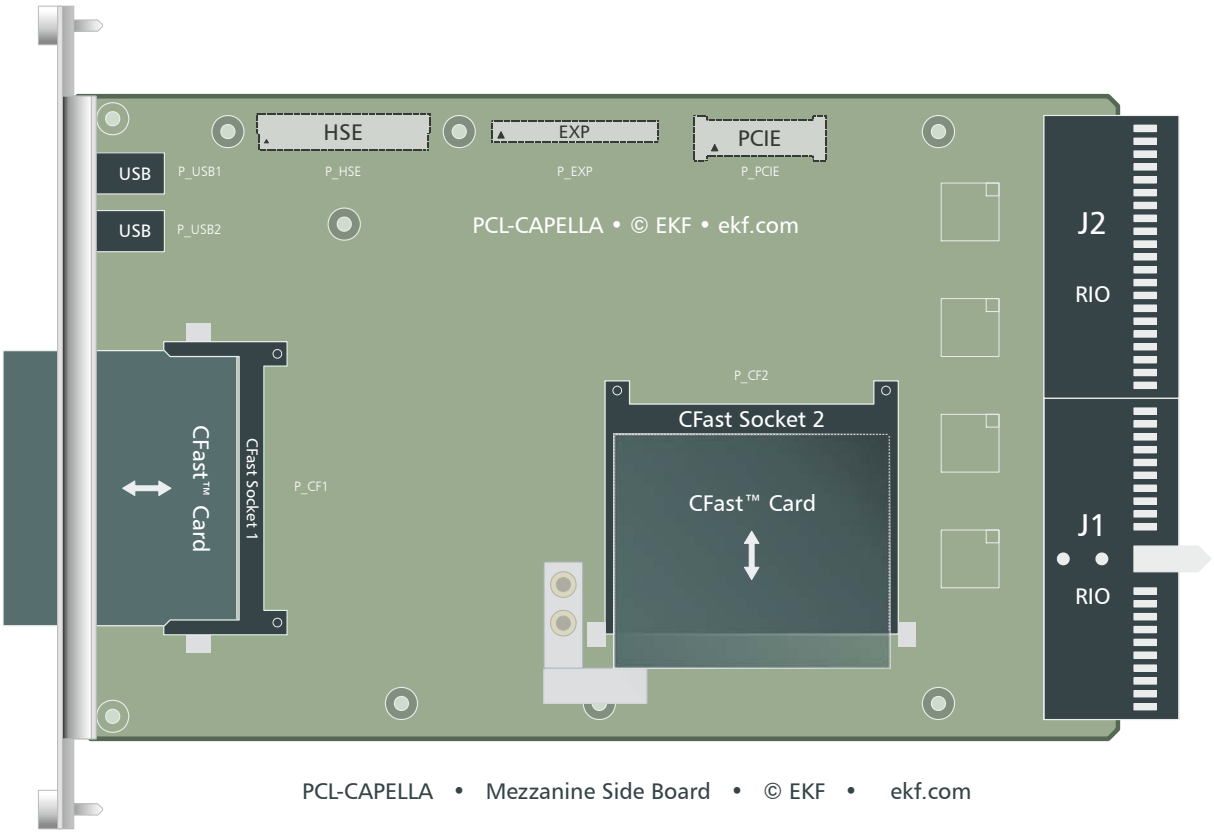
The connectors CF1/CF2 are discussed here, because CF1 is assigned to the front panel slot. While CF1 is wired to the SATA1 port derived from the mezzanine connector HSE, CF2 is tied to SATA4. Card guides ensure proper insertion of the CFast™ card, which would be fixed by a screw locked front panel latch (CF1), or a latching retainer respectively (CF2). The **card orientation must be top side** (card manufacturer label) **aligned right** with respect to the PCL-CAPELLA normal mounting position.

By default the front panel slot is dimensioned for 3.6mm card width (type I). A type II card (5.0mm) would require a modified front panel (please specify before ordering. Either a CFast™ Specification Rev. 1.1 or 2.0 compliant device is accepted.

The maximum data transfer rate would be limited by the SSD actually in use (refer to manufacturer datasheet), and by the CPU carrier card platform controller hub. With respect to the PC3-ALLEGRO CPU board, both SATA1 and SATA4 are 3G compliant SATA ports.

Both sockets are electrically equivalent. If two CFast™ cards are populated, they can be operated as RAID Level 0/1 array optionally (soft RAID with respect to PCH SATA controller).

CF1 (Front Panel) & CF2 (on-Board)



Population of CF2 is exclusive to MS1 only.

CF1/CF2 • CFast™ Host Connector • 218.5.024.21	
Part No. 218.5.024.21 • CFast™ Host Connector  © EKF • ekf.com	
S1	GND
S2	SATA1_TXP
S3	SATA1_TXN
S4	GND
S5	SATA1_RXN
S6	SATA1_RXP
S7	GND
PC1	*CDI*
PC2	GND
PC3	*DEVSLP*
PC4	*RSV*
PC5	*RSV*
PC6	*RSV*
PC7	GND
PC8	LED1 (PHYRDY Signal) 2)
PC9	LED2 (HDDA Signal) 2)
PC10	*RSV*
PC11	*RSV*
PC12	*IFDet*
PC13	+3.3V 1)
PC14	+3.3V 1)
PC15	GND
PC16	GND
PC17	*CDO*

gray/italic = NC

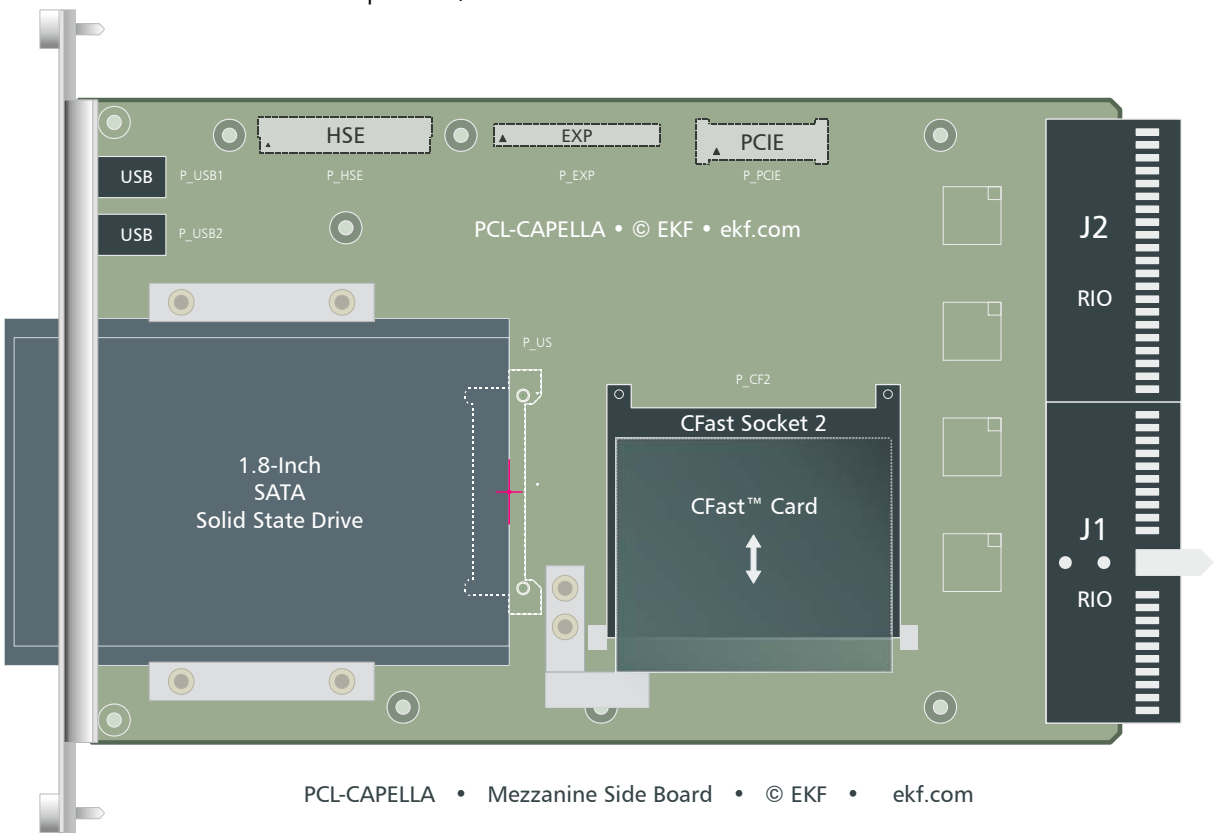
1) Overcurrent protected by 1.5A self resetting fuse (1200mA required by specification)
2) LED outputs deprecated by CFast™ 2.0 specification

Micro SATA

As an alternate (ordering option) to the CFast™ front panel connector CF1, the PCL-CAPELLA can be equipped with a host connector US1 for a front panel removable µSATA SSD. This is a 1.8-inch SATA drive according to the SFF-8144 specification, formerly popular in notebooks and other mobile devices, with dimensions of 5.0mm (typically) x 78.5mm x 54.0mm. The Micro SATA connector in use is defined in Serial ATA Rev. 2.6. Devices with 8.0mm height (probably mature hard disk) could be also used on the PCL-CAPELLA, but would require a modified front panel (consider before ordering).

Guide rails are used to hold the drive in its position, and in addition a screw locked front panel latch, sufficient for extremely rugged applications.

Option F/P Removable Micro SATA SSD



PCL-CAPELLA • Mezzanine Side Board • © EKF • ekf.com

US1 • Micro SATA Docking Connector 7+9 • 256.016.10.01		
	S1	GND
	S2	TX+ SATA1
	S3	TX- SATA1
	S4	GND
	S5	RX- SATA1
	S6	RX+ SATA1
	S7	GND
	P1	+3.3V
	P2	+3.3V
	P3	GND
	P4	GND
	P5	+5V
	P6	+5V
	P7	DAS (R to GND)
	P8	NC
	P9	NC

Signal designations RX/TX assigned with respect to the SATA host controller (PCH). Typical Micro SATA SSD devices are powered from a single +3.3V rail. Power is supplied (and switched on/off according to Sx state) from the CPU carrier board, across the mezzanine connectors.

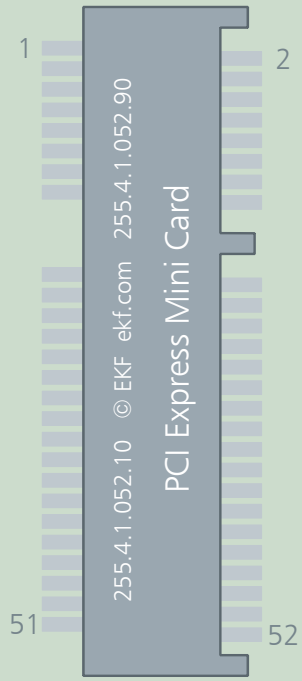
Intel® Micro SATA SSD

On-Board Connectors

mSATA Host Connector

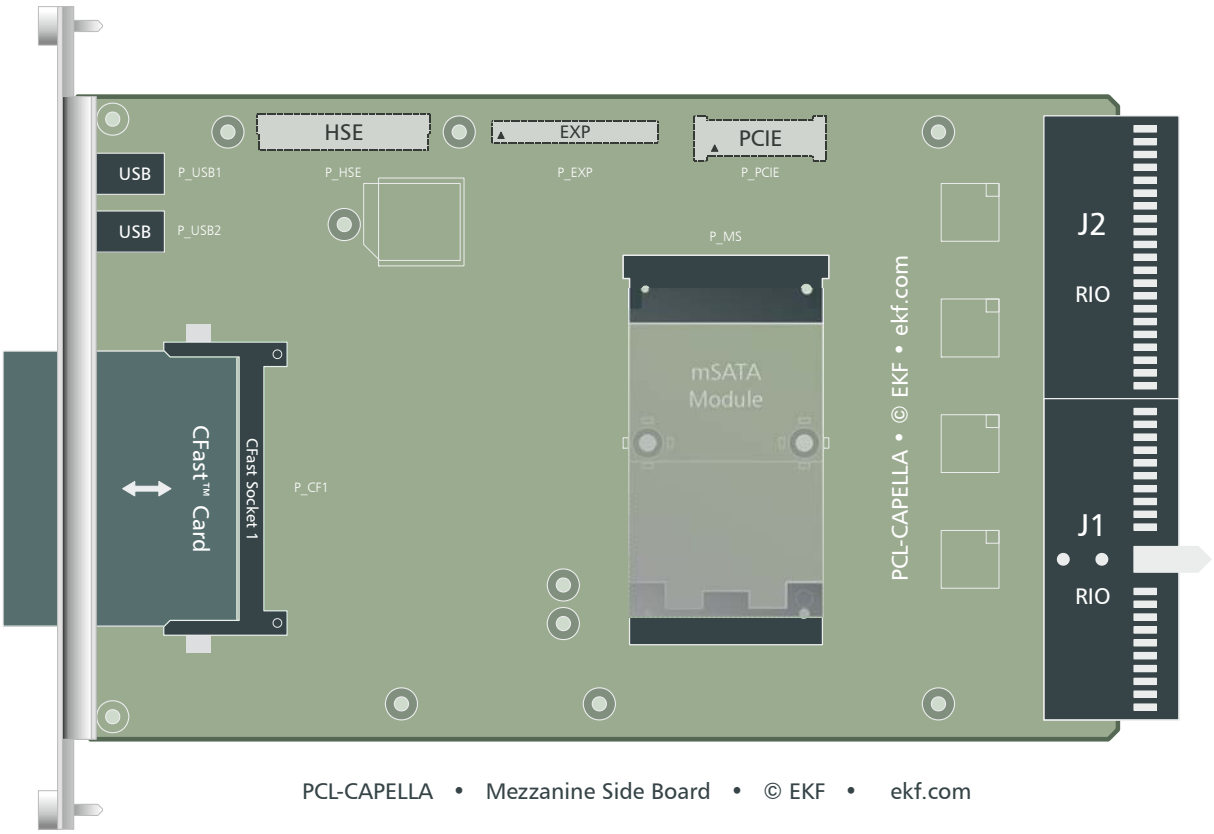
Optionally, the PCL-CAPELLA can be equipped with a mSATA module host connector MS1, for use with a mSATA SSD. After inserted, the mSATA card has to be fixed by a snap-in latch (full-size modules 50.80mm length), or will have to be secured manually by screws (mini size modules 26.80mm length), in order to withstand shock and vibration. Population of MS1 is exclusive to CF2 only.

MS1
mSATA / PCI Express® Mini Card Socket (255.4.1.052.10) & Latch (255.4.1.052.90)



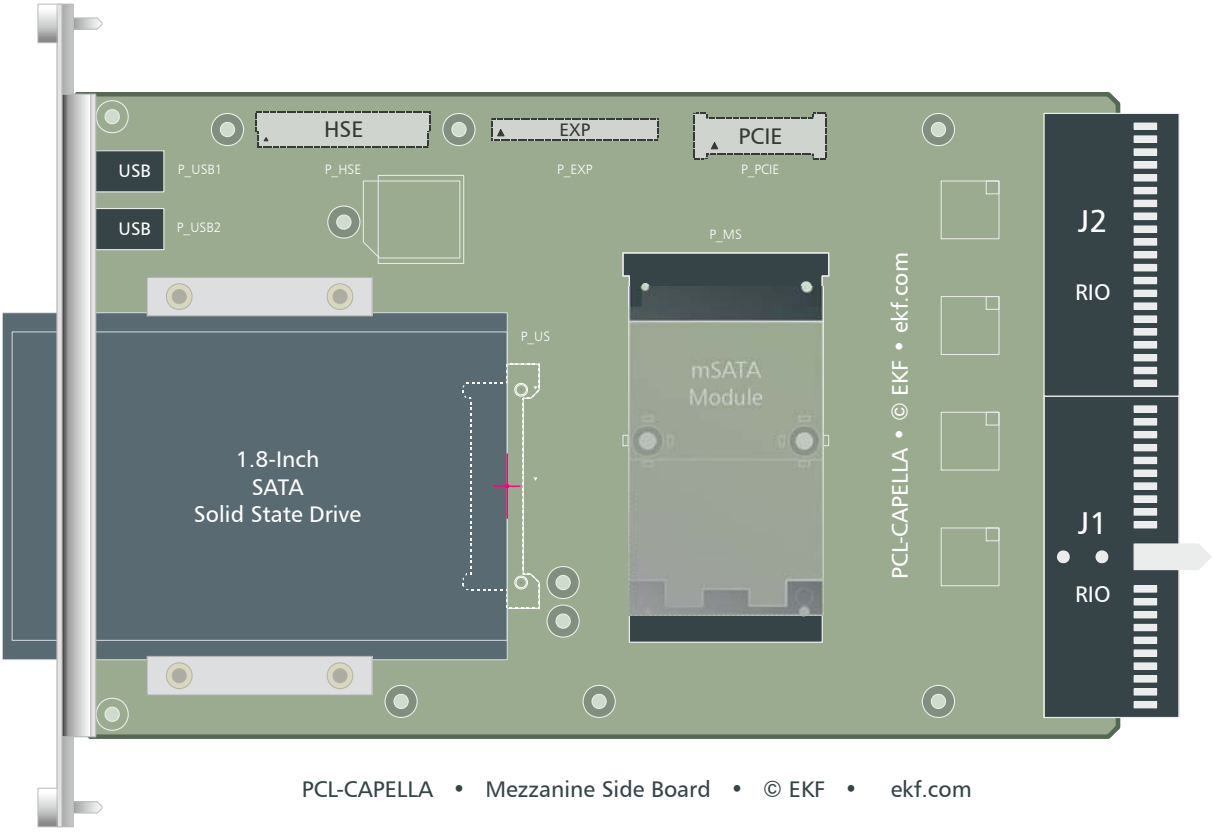
NC	1	2	+3.3V
NC	3	4	GND
NC	5	6	+1.5V
NC	7	8	NC
GND	9	10	NC
NC	11	12	NC
NC	13	14	NC
GND	15	16	NC
NC	17	18	GND
NC	19	20	NC
GND	21	22	NC
SATA_RXP (+B)	23	24	+3.3V
SATA RXN (-B)	25	26	GND
GND	27	28	+1.5V
GND	29	30	NC
SATA TXN (-A)	31	32	NC
SATA TXP (+A)	33	34	GND
GND	35	36	NC
GND	37	38	NC
+3.3V	39	40	GND
+3.3V	41	42	NC
NC	43	44	NC
NC	45	46	NC
NC	47	48	+1.5V
DA/DSS	49	50	GND
Presence	51	52	+3.3V

gray/italic = NC



PCL-CAPELLA • Mezzanine Side Board • © EKF • ekf.com

Option on-Board mSATA Module Connector



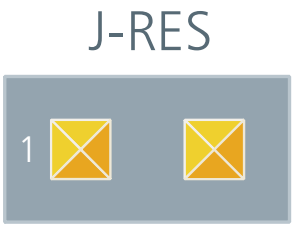
PCL-CAPELLA • Mezzanine Side Board • © EKF • ekf.com

Option on-Board mSATA Module Connector

On-Board Jumpers

J-RES Reset

Provided as an option, the pin header J-RES can be used for resetting the CPU host board (processor reset) if wired to additional circuitry (e.g. watchdog or manual pushbutton). Tie reset# to GND with an open collector output. While debugging the system, a 2.54mm jumper may be used to force a manual reset.



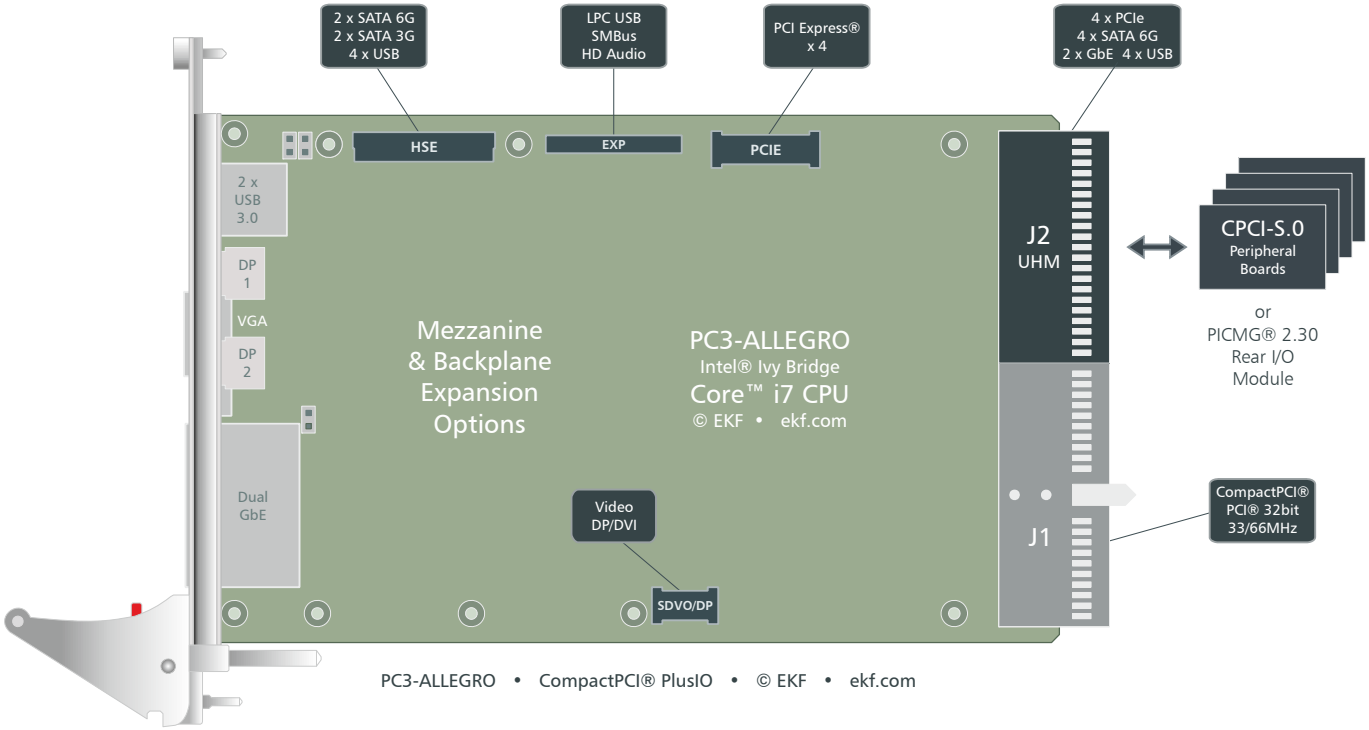
1=RST# 2=GND

no stuff by default

Inter-Board Connectors

The PCL-CAPELLA is equipped with 3 inter-board connectors. These are the EXP (LPC and mixed signals), the HSE (SATA & USB), and the PCIE (4-Lane PCI Express®)connectors. All host CPU inter-board connectors are situated at the bottom of the PCL-CAPELLA and establish the data path and power link to the carrier board CPU.

As the PCL-CAPELLA comes typically mounted as a unit together with the PC3-ALLEGRO or PC1-GROOVE (or other carrier board), there is normally no need for the user to get access to any of the inter-board connectors. They are described here as a reference only and for better understanding of the PCL-CAPELLA.



Related Information CPU Carrier Cards	
PC1-GROOVE (CompactPCI® PlusIO)	www.ekf.com/p/pc1/pc1.html
PC3-ALLEGRO (CpmpactPCI® PlusIO)	www.ekf.com/p/pc3/pc3.html

EXP	
I/F Type	PC3-ALLEGRO Controller
LPC (Low Pin Count)	PCH (Platform Controller Hub)
HD Audio	PCH (Platform Controller Hub)
SMBus	PCH (Platform Controller Hub)
2 x USB 2.0	PCH (Platform Controller Hub)

HSE	
I/F Type	PC3-ALLEGRO Controller
SATA01, SATA04 (3G)	PCH (Platform Controller Hub)
SATA02, SATA03 (6G)	PCH (Platform Controller Hub)
4 x USB 2.0	1:4 USB Hub

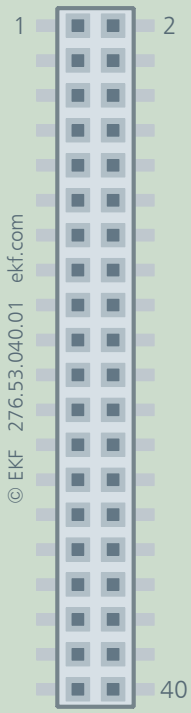
PCIE	
I/F Type	PC3-ALLEGRO Controller
PCI Express®	PE Switch

PCL-CAPELLA over PC3-ALLEGRO

EXP

The inter-board connector EXP is mounted on bottom of the PCL-CAPELLA PCB. This allows to attach the PCL-CAPELLA mezzanine companion card on top of the CPU carrier board. A suitable board stacker is used in addition to bridge the gap between the two boards (exactly 4HP distance between PCBs). EXP is used to pass the Low Pin Count I/F to the PCL-CAPELLA, besides two USB channels and some sideband signals.

EXP • Expansion Board Interface (LPC/HD-Audio/USB)
1.27mm Socket 2 x 20 (276.53.040.01)



1.27mm Socket

pin orientation shows CPU carrier board top view

GND	1	2	+3.3V_CR *
CLK_33MHZ	3	4	PLTRST#
LPC_AD0	5	6	LPC_AD1
LPC_AD2	7	8	LPC_AD3
LPC_FRAME#	9	10	LPC_DRQ#
GND	11	12	+3.3V_CR *
SERIRQ	13	14	PME#
SMI#	15	16	CLK_14MHZ
	17	18	
KBD_RST#	19	20	A20GATE
GND	21	22	+5V_CR *
USB2_DN	23	24	USB1_DN
USB2_DP	25	26	USB1_DP
USB_OC#	27	28	DBRESET#
SMB_CLK	29	30	SMB_DAT
GND	31	32	+5V_CR *
HDA_SDOUT	33	34	*HDA_SDIN0*
HDA_RST#	35	36	*HDA_SYNC*
HDA_BITCLK	37	38	
SPEAKER	39	40	+12V_A

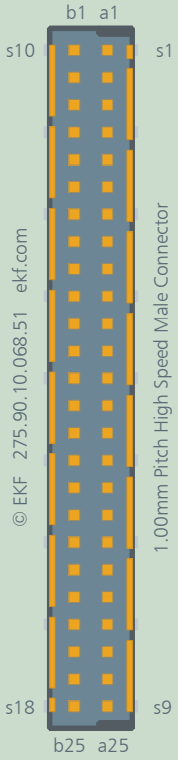
gray/italic = NC

* switched power supply lines from CPU carrier board according to Sx state

HSE

The connector HSE is a 10mm height shielded male pin header. Its counterpart on the CPU carrier board is a 8mm height receptacle, for a nominal headroom of 18.72mm between the boards (equivalent to 4HP board to board CL pitch).

HSE • SATA & USB Mezzanine Interface
1.00mm Pitch Male Connector 10mm Height (275.90.10.068.51)



GND	b1	a1	GND
SATA03_TXP 4)	b2	a2	SATA01_TXP 3)
SATA03_TXN 4)	b3	a3	SATA01_TXN 3)
GND	b4	a4	GND
SATA03_RXN 4)	b5	a5	SATA01_RXN 3)
SATA03_RXP 4)	b6	a6	SATA01_RXP 3)
GND	b7	a7	GND
SATA04_TXP 3)	b8	a8	SATA02_TXP 4)
SATA04_TXN 3)	b9	a9	SATA02_TXN 4)
GND	b10	a10	GND
SATA04_RXN 3)	b11	a11	SATA02_RXN 4)
SATA04_RXP 3)	b12	a12	SATA02_RXP 4)
GND	b13	a13	GND
USB3_P	b14	a14	USB1_P
USB3_N	b15	a15	USB1_N
GND	b16	a16	GND
USB4_P	b17	a17	USB2_P
USB4_N	b18	a18	USB2_N
GND	b19	a19	GND
USB3_OC#	b20	a20	USB1_OC#
USB4_OC#	b21	a21	USB2_OC#
+5V_CR 2)	b22	a22	+3.3V_CR 1)
+5V_CR 2)	b23	a23	+3.3V_CR 1)
+5V_A	b24	a24	+3.3V_A
+12V_A	b25	a25	+12V_A

1) 2) Switched voltages from carrier board, according to CPU sleep state S0
3) 3Gbps SATA (PC3-ALLEGRO)
4) 6Gbps SATA (PC3-ALLEGRO)

Notes:
- All s# connector pins (shield) are tied to GND
- All TX/RX designations with respect to SATA controller (TX controller = RX drive, RX controller = TX drive)

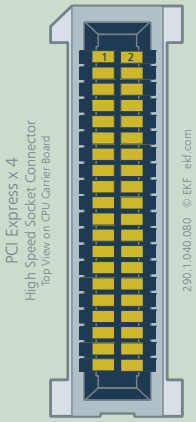
PCIE

The high speed expansion socket PCIE is mounted on bottom of the PCL-CAPELLA. This allows to attach the mezzanine companion card on top of the CPU carrier board. A mating strip line spacer PCB (C22-PCIEX2) is used in addition to bridge the gap between the two boards, which results from the horizontal 0.8-inch (20.32mm) card slot pitch.

PCIE must be organized as 4 links by 1 lane each (i.e. 4 single PCI Express® lanes). Check the CPU carrier card PCIE DIP-switch settings for proper configuration

PC1-GROOVE:	DSW1.1 = OFF	DSW1.2 = ON
PC3-ALLEGRO:	DS-P.1 = OFF	DS-P.2 = ON

PCIE • PCI Express x 4
High Speed Dual Row Socket 0.8mm Pitch 290.1.040.080



pin assignment shows CPU carrier board top view (see-trough mezzanine side board PCB)

[1] switched on/off power lines on CPU carrier boards according to S3 state

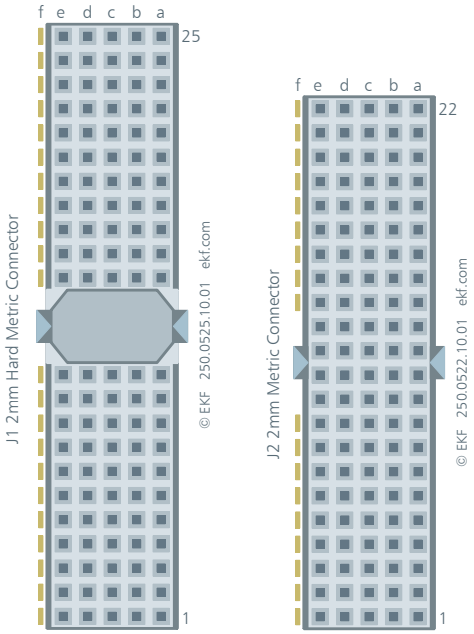
GND	1	2	GND
+5V_CR [1]	3	4	+3.3V_CR [1]
+5V_CR [1]	5	6	+3.3V_CR [1]
GND	7	8	GND
PE_CLKP	9	10	PLTRST#
PE_CLKN	11	12	*PE_WAKE#*
GND	13	14	GND
PE0_TP	15	16	PE0_RP
PE0_TN	17	18	PE0_RN
GND	19	20	GND
GND	21	22	GND
PE1_TP	23	24	PE1_RP
PE1_TN	25	26	PE1_RN
GND	27	28	GND
PE2_TP	29	30	PE2_RP
PE2_TN	31	32	PE2_RN
GND	33	34	GND
PE3_TP	35	36	PE3_RP
PE3_TN	37	38	PE3_RN
GND	39	40	

[1] Supply voltages from carrier board, switched on/off according to sleep state

Rear I/O Connectors

As an option together with CompactPCI® and CompactPCI® PlusIO CPU carrier cards only, the PCL-CAPELLA can be equipped with the rear I/O connectors J1 and J2. A single slot rear I/O backplane (directly adjoining the CPCI backplane) would be required for handing over the available signal lines to a suitable rear I/O transition module. A single slot P1/P2 backplane however does not fit into a system with a left hand CPCI Serial backplane (4HP slot distance).

The PCL-CAPELLA must not be plugged into a common CompactPCI® peripheral slot in order to avoid damaging the board or other components of the system. A brown key on the J1 connector will prevent the user from erroneously inserting the PCL-CAPELLA into an unsuitable position.



Signal names used in the J1 and J2 connector tables hereafter are associated with their main function. However, the Super I/O controller allows a number of signals also be used as general purpose I/O. Please consult the SMSC SCH3114 datasheet for details (www.microchip.com).

J1 is used for three groups of high speed signals, i.e. SATA, USB, and Gigabit Networking. For proper operation, a suitable termination circuitry would be required on a rear I/O module. Please contact EKF for schematic details, if RIO design is intended by the customer itself (support@ekf.com).

With respect to the networking interface controllers, magnetics modules are mandatory on a RIO module, or equivalent RJ-45 jacks with integrated magnetics. In order to avoid compatibility issues for customers who want to migrate from a CCL-CAPELLA side card, the PCL-CAPELLA is equipped with the proven Intel® 82574IT GbE controllers (launch 2008). These components may be replaced on the PCL-CAPELLA ~2018 by the Intel® i210IT (launch 2012), or even more recent parts.

J1

Connector Assignment J1 Rear I/O

J1	A	B	C	D	E
25	+5V_S		+1.9V (Ethernet)	+3.3V_S	+5V_S
24	NIC1_MX0+	GND	NIC1_MX1+	NIC1_MX2+	NIC1_MX3+
23	NIC1_MX0-	GND	NIC1_MX1-	NIC1_MX2-	NIC1_MX3-
22	NIC2_MX0+	GND	NIC2_MX1+	NIC2_MX2+	NIC2_MX3+
21	NIC2_MX0-	GND	NIC2_MX1-	NIC2_MX2-	NIC2_MX3-
20	GND	GND	GND	GND	GND
19	NIC3_MX0+	GND	NIC3_MX1+	NIC3_MX2+	NIC3_MX3+
18	NIC3_MX0-	GND	NIC3_MX1-	NIC3_MX2-	NIC3_MX3-
17	GND	GND	GND	GND	GND
16	NIC4_MX0+	GND	NIC4_MX1+	NIC4_MX2+	NIC4_MX3+
15	NIC4_MX0-	GND	NIC4_MX1-	NIC4_MX2-	NIC4_MX3-
14	KEY AREA - BROWN KEY				
13					
12					
11	SATA2_TP 2)	GND		USB1_HSE_DM 1)	USB1_HSE_OC# 1)
10	SATA2_TN 2)	GND		USB1_HSE_DP 1)	
9	100nF to GND	100nF to GND	GND	100nF to GND	100nF to GND
8	SATA2_RN 2)	GND	GND	USB2_HSE_DM 1)	USB2_HSE_OC# 1)
7	SATA2_RP 2)	GND	GND	USB2_HSE_DP 1)	GND
6	GND	GND		GND	
5	SATA3_TP 2)	GND			
4	SATA3_TN 2)	GND	GND	100nF to GND	GND
3	GND	GND			
2	SATA3_RN 2)	GND			
1	SATA3_RP 2)	GND	GND	GND	GND

1) Rear I/O USB ports as provided by mezzanine connector HSE
2) Rear I/O SATA channels as provided by mezzanine connector HSE

Power pins: *_S = switched on/off according to CPU carrier card sleep state
*_A = always on (if system power on)

J2

Connector Assignment J2 Rear I/O

J2	A	B	C	D	E
22	+5V_S	+3.3V_S			+12V_S
21	GND	GND	GND	GND	GND
20	SP1_RI#	SP1_CTS#	SP2_RI#/GP50	SP2_CTS#/GP56	
19	SP1_RXD	GND	SP2_RXD/GP52	GND	
18	SP1_DSR#	SP1_DCD#	SP2_DSR#/GP54	SP2_DCD#/GP51	
17	SP1_DTR# 3)	GND	SP2_DTR#/GP57	GND	GND
16	SP1_RTS# 3)	SP1_TXD	SP2_RTS#/GP55 3)	SP2_TXD/GP53	RESET_IN#
15		GND		GND	RESET_OUT#
14	SP3_RI#/GP13	SP3_CTS#/GP16	SP4_RI#/GP31	SP4_CTS#/GP62	SMB_DAT 1)
13	SP3_RXD/GP10	GND	SP4_RXD/GP64	GND	SMB_CLK 1)
12	SP3_DSR#/GP14	SP3_DCD#/GP12	SP4_DSR#/GP66	SP4_DCD#/GP63	GND
11	SP3_DTR#/GP15	GND	SP4_DTR#/GP34 2)	GND	USB1_EXP_DM 5)
10	SP3_RTS#/GP17	SP3_TXD/GP11	SP4_RTS#/GP67 2)	SP4_TXD/GP65	USB1_EXP_DP 5)
9		GND		GND	GND
8	LPT_SLCT	LPT_PE	LPT_BUSY	SIO_GP47	USB_EXP_OC# 5)
7	LPT_ACK#	GND	GND	SIO_GP46	GND
6	LPT_D7	LPT_D6	LPT_D5	SIO_GP45	USB2_EXP_DM 5)
5	LPT_D4	GND	LPT_D3	SIO_GP44	USB2_EXP_DP 5)
4	LPT_D2	LPT_D1	LPT_SLCTIN#	SPEAKER	GND
3	LPT_D0	GND	LPT_INIT#	KBDAT	KBCLK
2	LPT_ALF#	LPT_ERROR#	LPT_STROBE#	GND	+5V_S
1	GND	GND	GND	MSDAT	MSCLK

1) Manufacturing option: SM Bus signals buffered via LTC4300A-3, voltage level @ +5V_CR, buffer enable input is controlled by GP40 SCH3114 SIO (high=enabled)
2) GP34 may be used to control serial EEPROM A1 (stuffing option)
GP67 may be used to control serial EEPROM WP (stuffing option)
3) These serial port handshake signals may be also in use for power up strapping options of the SCH3114 SIO (10k PU or PD) with no or minor impact on normal operation
4) 3.3V compliant GPIOs derived from the TUSB7320/TUSB7340 USB 3.0 SuperSpeed host controller (10k PU)
5) Rear I/O USB ports as provided by mezzanine connector EXP

Additional Functions

SMBus EEPROM

The PCL-CAPELLA is provided with a 24C02 2Kbit I^2C EEPROM, for storing board configuration data. The EEPROM is accessed via the SMBus.

If required, the SMBus EEPROM address A1 can be optionally controlled (stuffing option) by SIO GP34 (serial port 4 DTR#), and the SMBus EEPROM WP is likewise tied to GP67 (serial port 4 RTS4#).

Schematics

Complete circuit diagrams for this product are available for customers on request. Signing of a non-disclosure agreement would be needed. Please contact sales@ekf.de for details.

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